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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,019	HO ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,19-22 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,19-22 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

In view of the amendment filed on 11/23/2005, the Examiner withdraws the claim objections to claim 12 of the previous Office Action.

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

Applicant's arguments filed on 11/23/2005 have been fully considered but they are not persuasive.

Regarding claims 19-22 for Non-Enablement:

Applicant's arguments with respect to claims 19-22 have been considered but are moot in view of the new ground(s) of rejection under 35 USC 112 first paragraph as filing to comply with the written description requirement.

Regarding claim 27 for Non-Enablement:

Applicant's arguments with respect to claim 27 have been considered but are moot in view of the new ground(s) of rejection under 35 USC 112 first paragraph as filing to comply with the written description requirement.

Regarding The Examiner's "Response to Argument":

The Applicant contends, "Applicants asserts that this evidences that claim 1 is not anticipated by the teachings of the McCormack et al. reference "

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, as per claim 1 McCormack discloses a crosspoint switch integrated circuit comprising an array of input ports (figure 1 block 301 page 2 paragraph [0037]); an array of output ports (figure 1 block 303 page 2 paragraph [0037]); a switch matrix configured to selectively connect the input ports to the output ports for conducting electrical signals therebetween (figure 1 block 101 page 2 paragraph [0037]); and equalization circuitry coupled to at least partially offset transmission losses experienced by the electrical signal while external to the crosspoint switch integrated circuit (figure 1 block 201 page 2 paragraph [0037]) the equalization circuitry is configured to measure jitter within the electrical signals and to utilize jitter measurements as a basis for offsetting the transmission losses, the equalization circuitry being adaptive circuitry enabled to automatically select levels of equalization (figure 1 block 201 page 1 paragraph [0008] page 2 paragraph [0037] and page 4 paragraph [0054]). AS per claim 19 As per claim 19 McCormack discloses a method of providing equalization for a crosspoint formed on an integrated circuit chip switch comprising determining signal characteristics related to signal transmissions via each of a plurality of ports of the crosspoint switch (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0051] to [0056]), including providing on-chip measurements of jitter of electrical signals, (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0051] to [0060]), where the jitter is induced by off-chip conditions (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0053] and [0051] to [0056]); and setting equalization circuitry housed within the crosspoint switch such that each the port has filtering

characteristics tailored on a basis of the signal characteristics for the signal transmissions via the each port the setting being automated and being at least partially based on on-chip measurements of jitter (figure 2 block 21 page 4 paragraphs [0051] to [0060]).

Paragraph **[0037]** discloses, " FIG. 1 illustrates a block diagram of one embodiment of a switch of the present invention. The switch includes a switch core 101, a switch configuration register 103, a staging register 105, and a programming interface 109. In somewhat more detail, the switch core couples signals from an input bus 301 to an output bus. The switch configuration register determines which output signals of the output bus are derived from which signals of the input bus. The staging register provides a temporary programming register, the contents of which are transferred to the switch configuration register when remapping of the outputs to the inputs is desired. The staging register is accessed using the programming register. The input bus provides a number of signals each to input signal equalization circuits 201. The input equalization circuits are coupled to the switch core. Similarly, outputs of the switch core are coupled to output level control circuits 203 which are coupled to an output bus 303. As such, data transmitted on the input bus is transferred to the output bus via the input signal equalization circuits, the switch core and the output level control circuits".

Paragraph [0008] discloses "When the data pulse passes a given threshold level, a pattern-dependant jitter occurs. The pattern-dependant jitter is often due to the narrowing or widening of the data pulses that depends on the data pulses' voltage history. A signal that has been distorted in this way is difficult to recover error-free."; and

paragraph [0054] "**since the network includes passive elements, these elements can be segmented and/or programmable (i.e., tunable)**. For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for **easy tuning of a circuit's ISI jitter characteristics**". For these reasons and the reasons indicated in the previous Office Action the rejection of claims 1 and 19 are maintained.

Regarding Patentability of claims 25 and 26:

The Applicant contends, "It is further asserted that neither Fig. 11 nor paragraphs [0081]-[0084] of McCormack et al. teaches a multiplexer operatively associated with a jitter measurement component to enable jitter measurement on a port-by-port basis. "

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, admitted prior art in paragraph [0002] discloses "A crosspoint switch may be used to dynamically connect any one of a number of input channels to any one or more of a number of output channels. The crosspoint switch may be a single integrated circuit chip having an array of input ports and an array of output ports. For example, there may be 68 input ports and 68 output ports. Each output port has a dedicated multiplexer which is linked to all of the input ports, so that an incoming signal at an input port can be routed to a selected output port, a group of selected output ports, or all of the output ports. The routing of the signals by the crosspoint switch multiplexers is controlled by operations of address registers. In the example in which there are 68 input ports, the crosspoint switch will have 68 address registers or register pairs, since there is an

address register dedicated to each multiplexer". McCormack discloses how it can be selected individual input and individual output of the circuits "In one embodiment drive and sense functions are also provided. The drive function drives an input line of the switch fabric to a specified state. The sense function senses the state of a an output line of the switch fabric" and also output elements "Similarly, an output drive line is provided for the outputs of the switch. The output drive line is multiplexed with the output signal approximate the output signal driver, with the output signal driver outputting either an output data signal or the signal on the output drive line based on contents of the switch configuration register"; and as indicated previously McCormack also discloses "**since the network includes passive elements, these elements can be segmented and/or programmable (i.e., tunable)**. For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for **easy tuning of a circuit's ISI jitter characteristics**". For these reasons and the reasons indicated in the previous Office Action the rejection of claim 25 is maintained.

The Applicant contends, "Neither Blazo et al. nor McCormack et al. teaches or suggests providing a crosspoint switch integrated circuit having a jitter measurement component of any type. Moreover, neither reference provides the description or suggestion of the multiplexer used in the manner described in claim 25 with respect to equalization circuitry of a crosspoint switch integrated circuit. Without a reading of Applicants' disclosure, there would be no motivation In combining the teachings of the prior art in the manner described in the pending claims."

The Examiner disagrees and asserts, that, as indicated in the previous Office Action McCormack discloses claim 25. McCormack doesn't disclose a jitter measurement component includes a phase-locked loop for tracking data transactions within electrical signals, the jitter measurement component including a voltage-controlled oscillator connected to be responsive to operations of the phase locked loop. Blazo discloses a jitter measurement component includes a phase-locked loop for tracking data transactions within electrical signals, the jitter measurement component including a voltage-controlled oscillator connected to be responsive to operations of the phase locked loop (figure 1 column 3 lines 36-50). McCormack and Blazo are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the jitter measurement circuit disclosed by Blazo. The suggestion/motivation for doing so would have been to measure jitter at low frequencies (Blazo abstract and lines 36-50). For these reasons and the reasons indicated in the previous Office Action the rejection of claim 26 is maintained.

Regarding Patentability of claim 27:

The Applicant contends, "Clearly, block 21 in Fig. 2 of McCormack et al. does not show jitter measurements. The block merely shows three resistors and two capacitors. The block is a pre-compensation network. The cited paragraphs describe the network, but do not described on-chip jitter measurements and do not describe recurring executions of such measurements.".

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, McCormack also discloses that the equalization circuit is configured to recurringly execute jitter measurements and recurringly execute responsive selection of levels of equalization for individual input ports, enabling levels of equalization to track variations in transmission losses (figure 2 block 21 and figure 4 paragraphs [0054] to [0057]). Paragraph [0054] indicates "since the network includes passive elements, these elements can be segmented and/or **programmable** (i.e., tunable). For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for **easy tuning of a circuit's ISI jitter characteristics.** In one embodiment, the elements of the network are tuned, such that it compensates for all or some of the signal degradation occurring in the transmission medium leading up to a crosspoint switch device. This is particularly valuable in applications where multiple stages of crosspoint switch devices are cascaded to form a large switch fabric having grossly non-ideal electrical or electro-optical connections between the switch devices. Thus, placing a network of the present invention between each of the cascaded crosspoint switch devices reduces signal degradation.

In one embodiment, referring back to FIG. 2, at point X1 between the capacitor C1 and the resistor RS1, a first input transmission line is coupled to the network. At point X2, between the capacitor C2 and the resistor RS2, a second input transmission line is coupled to the network. At point Y1, between the capacitor C1, the resistor RS1 and resistor RP1, a first transmission line of the first set of transmission lines is coupled

to the network. Likewise, at point Y2, between the capacitor C2, the resistor RS2 and resistor RP1, a second transmission line of the first set of transmission lines is coupled to the network. Although only one transmission line is described above coupled to each point X1, X2, Y1 and Y2, multiple transmission lines can be coupled to the points.

The switch matrices in one embodiment also include output pre-emphasis circuitry. The output pre-emphasis circuitry is adapted to drive signals over loads, with decreased reduction of higher frequency components of the signal. FIG. 4 is a semi-schematic of output pre-emphasis circuit providing differential outputs of the switch matrices. The circuit is comprised of a first capacitively coupled differential pair and a second differential pair. The capacitive element coupling the first differential pair is selectable, i.e. tunable. In one embodiment this is accomplished using an array of selectable capacitors in series or in parallel, selectable using register bits. A resistive element also coupled between the first differential pair, and the resistive element is similarly selectable.". For these reasons and the reasons indicated in the previous Office Action the rejection of claim 27 is maintained.

Regarding claims 7 and 21:

The Applicant contends, "Yiu was cited for disclosing switchable connections arranged in electrical parallel and components that include inductors and resistors. Applicants assed that even if one were to modify McCormack et al. to include sue switchable connections, the resulting device and method would render Independent claims 1 and 19 obvious under Section 103(a).".

The Examiner disagrees and asserts, that, as indicated in the previous Office Action, McCormack doesn't disclose that the switchable connections are arranged in electrical parallel and the components include an inductor and a resistor. Yiu discloses that the switchable connections are arranged in electrical parallel and the components include an inductor and a resistor (figures 3 and 8 column 6 lines 27-45). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). For these reasons and the reasons indicated in the previous Office Action the rejection of claims 7 and 21 are maintained.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 19-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification doesn't disclose that "the jitter is induced by off-chip conditions".

Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification doesn't disclose that "recurringly execute said jitter measurement and recurringly execute responsive selection of said levels of equalization".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-6, 8, 9, 12, 14, 19, 20 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by McCormack (US Patent Publication 20020020905 A1).

As per claim 1 McCormack discloses a crosspoint switch integrated circuit comprising an array of input ports (figure 1 block 301 page 2 paragraph [0037]); an array of output ports (figure 1 block 303 page 2 paragraph [0037]); a switch matrix configured to selectively connect the input ports to the output ports for conducting electrical signals therebetween (figure 1 block 101 page 2 paragraph [0037]); and equalization circuitry coupled to at least partially offset transmission losses experienced

by the electrical signal while external to the crosspoint switch integrated circuit (figure 1 block 201 page 2 paragraph [0037]) the equalization circuitry is configured to measure jitter within the electrical signals and to utilize jitter measurements as a basis for offsetting the transmission losses, the equalization circuitry being adaptive circuitry enabled to automatically select levels of equalization (figure 1 block 201 page 1 paragraph [0008] page 2 paragraph [0037] and page 4 paragraph [0054]).

As per claim 3 McCormack discloses the equalization circuitry includes a plurality of adjustable equalizers, the adjustable equalizers each having adjustable filtering characteristics within a fixed number of equalization settings (figure 2 block 21 page 4 paragraphs [0051] to [0056]).

As per claim 4 McCormack discloses that each the adjustable equalizer includes a plurality of switchable connections which individually adjust the filtering characteristics when activated (figure 4 page 4 paragraph [0057]).

As per claim 5 McCormack discloses that each the switchable connection includes a switch, at least some of the switchable connections including at least one component which significantly affects the filtering characteristics when the switchable connections are individually activated (figure 4 page 4 paragraph [0057]).

As per claim 6 McCormack discloses that at least some of the switchable connections are arranged in electrical parallel and the components include capacitors and resistors (figure 4 page 4 paragraph [0057]).

As per claim 8 McCormack discloses that the switches are transistors and the components include at least some of resistors, capacitors, or inductors (figure 4 page 4 paragraph [0057]).

As per claim 9 McCormack discloses that the adjustable equalizers are coupled to the input ports in one-to-one correspondence (figure 2 block 21 page 4 paragraphs [0051] to [0056] and figure 4 page 4 paragraph [0057]).

As per claim 12 McCormack discloses a crosspoint switching arrangement comprising a plurality of input ports connected to channels having non-uniform frequency responses with respect to incoming signal transmissions (figure 1 block 301 page 2 paragraph [0037]); a plurality of output ports connected to channels having non-uniform frequency responses with respect to outgoing signal transmissions (figure 1 block 303 page 2 paragraph [0037]); a switch matrix enabled to dynamically reconfigure connections of the input ports to the output ports (figure 1 block 101 page 2 paragraph [0037]); and equalization circuitry coupled to one of the input and output ports, the equalization circuitry including a separate equalization circuit for each channel for which equalization is to be applied, each equalization circuit having a plurality of available configurations of equalization, where selection of one of the available configurations for a particular equalization circuit establishes (figure 2 paragraphs [0049]-[0056] and figure 4 page 4 paragraph [0057]) filtering characteristics that are tailored on a basis of the frequency responses of the channels to which the specific ones of the input and output ports are connected, each equalization circuit being dedicated to a particular channel (figure 1 block 201 page 2 paragraph [0037]; figure 2 paragraphs [0049]-[0056] and

figure 4 page 4 paragraph [0057]);where said crosspoint switching arrangement is an integrated circuit having input ports, output ports, switch matrix and equalization circuit (paragraphs [0037], [0046] and [0054]).

As per claim 14 McCormack discloses a memory configured to store equalization settings for the equalization circuitry, the equalization settings stored at the memory including a selection of a particular available the configuration for each the equalization circuit (figure 4 page 4 paragraph [0057] and [0060]).

As per claim 19 McCormack discloses a method of providing equalization for a crosspoint formed on an integrated circuit chip switch comprising determining signal characteristics related to signal transmissions via each of a plurality of ports of the crosspoint switch (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0051] to [0056]), including providing on-chip measurements of jitter of electrical signals, (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0051] to [0060]), where the jitter is induced by off-chip conditions (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0053] and [0051] to [0056]); and setting equalization circuitry housed within the crosspoint switch such that each the port has filtering characteristics tailored on a basis of the signal characteristics for the signal transmissions via the each port the setting being automated and being at least partially based on on-chip measurements of jitter(figure 2 block 21 page 4 paragraphs [0051] to [0060]).

As per claim 20 McCormack discloses selectively activating and deactivating switching devices which introduce parallel connections of resistances and capacitances

within the adjustable equalization circuitry, the equalization circuitry being a plurality of adjustable equalization circuits (figure 4 page 4 paragraph [0057]).

As per claim 22 McCormack discloses activating adaptive equalization circuitry (figure 2 block 21 page 4 paragraphs [0051] to [0056]).

As per claim 25 McCormack discloses claim 1 McCormack also discloses that the equalization circuit includes a multiplexer connected to a jitter measurement component for providing said jitter measurements, said multiplexer being connected to receive said electrical signals from each of said input ports and being operatively associated with said jitter measurement component to enable the jitter measurement on a port-by-port basis (figure 11 paragraph [0080]-[0084]. The use of multiplexer is also admitted prior art in the specification see [0002] and [0010]).

As per claim 27 McCormack discloses claim 1 McCormack also discloses that the equalization circuit is configured to recurringly execute jitter measurements and recurringly execute responsive selection of levels of equalization for individual input ports, enabling levels of equalization to track variations in transmission losses (figure 2 block 21 and figure 4 paragraphs [0054] to [0057]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 15-18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack (US Patent Publication 20020020905 A1) as applied to claims 5, 12, 15-19 above, and further in view of Yiu (US 6104750 A).

As per claim 7 McCormack discloses claim 5. McCormack discloses that the tap, therefore, includes a capacitance and inductance (page 3 paragraph [0044]). McCormack doesn't disclose that the switchable connections are arranged in electrical parallel and the components include an inductor and a resistor. Yiu discloses that the switchable connections are arranged in electrical parallel and the components include an inductor and a resistor (figures 3 and 8 column 6 lines 27-45). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 7.

As per claim 15 McCormack discloses claim 12. McCormack discloses that each the equalization circuit includes a default configuration of first connected circuit components and a plurality of alternative configurations, the default configuration achieving a first level of frequency-dependent compensation (figure 2 block 21 page 4 paragraphs [0051] to [0056]). McCormack doesn't disclose the compensation for effects of skin loss in signals conducted via the channels. Yiu discloses the compensation for

effects of skin loss in signals conducted via the channels (figure 4A column 4 line 66 to column 5 line 8). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 15.

As per claim 16 McCormack and Yiu disclose claim 15. Yiu also discloses that each of the alternative configuration introduces second connected circuit components to achieve different levels of frequency-dependent compensation for the effects of skin loss (figure 4A and figures 3 and 8 column 4 line 66 to column 5 line 8 and column 6 lines 27-45). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 16.

As per claim 17 McCormack and Yiu disclose claim 16. McCormack also discloses that the second connected circuit components are coupled to switches that selectively introduce the second connected circuit components, the switches being

manipulated based upon the equalization settings stored in the memory (figure 4 page 4 paragraph [0057]). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 17.

As per claim 18 McCormack and Yiu disclose claim 17. McCormack also discloses that the equalization circuits are coupled to the input ports and are individually adjustable from an exterior of an integrated circuit chip package in which the equalization circuits and switch matrix reside (figure 2 block 21 page 4 paragraphs [0051] to [0056]). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 18.

As per claim 21 McCormack discloses claim 19. McCormack discloses selectively activating and deactivating switching devices (figure 4 page 4 paragraph [0057]). McCormack doesn't disclose series connections of resistances and inductances

within the adjustable equalization circuits. Yiu discloses series connections of resistances and inductances within the equalization circuits (figures 3 and 8 column 6 lines 27-45). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 21.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack (US Patent Publication 20020020905 A1) as applied to claim 25 above, and further in view of Blazo (US 5757652 A). McCormack discloses claim 25. McCormack doesn't disclose a jitter measurement component includes a phase-locked loop for tracking data transactions within electrical signals, the jitter measurement component including a voltage-controlled oscillator connected to be responsive to operations of the phase locked loop. Blazo discloses a jitter measurement component includes a phase-locked loop for tracking data transactions within electrical signals, the jitter measurement component including a voltage-controlled oscillator connected to be responsive to operations of the phase locked loop (figure 1 column 3 lines 36-50). McCormack and Blazo are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by

McCormack the jitter measurement circuit disclosed by Blazo. The suggestion/motivation for doing so would have been to measure jitter at low frequencies (Blazo abstract and lines 36-50). Therefore, it would have been obvious to combine McCormack with Blazo to obtain the invention as specified in claim 25.

Conclusion

Applicant's amendment filed on 9/1/2005 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

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12-05-2005

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